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(54) Abstract Title
High frequency analyser

(57) A method or means of measuring the response of an electronic device to a high (radio or microwave) frequency input signal from a source 2 comprises connecting two ports 3, 4 of the device to respective inputs to a measuring unit 10. Applying one or more input signals to the device and measuring the waveform from each respective port 3, 4. A time reference signal is supplied to a different input of the measurement unit to that of an input which is switching its signal source and processing measurements so as to maintain a time reference during the switching process. The above said measurements and calibration data are used to obtain absolute values of the magnitude and phase of the waveforms at the first and/or second port 3, 4 of the device. The measuring unit may include a microwave transition network analyser 10 and the switching of signals may be via switches SA, SB, SC, SD. A power splitter 14, phase shifters 17, variable amplifiers 18 and isolators 19 may be used to adjust the principle and harmonic frequency load pull applied to the device.
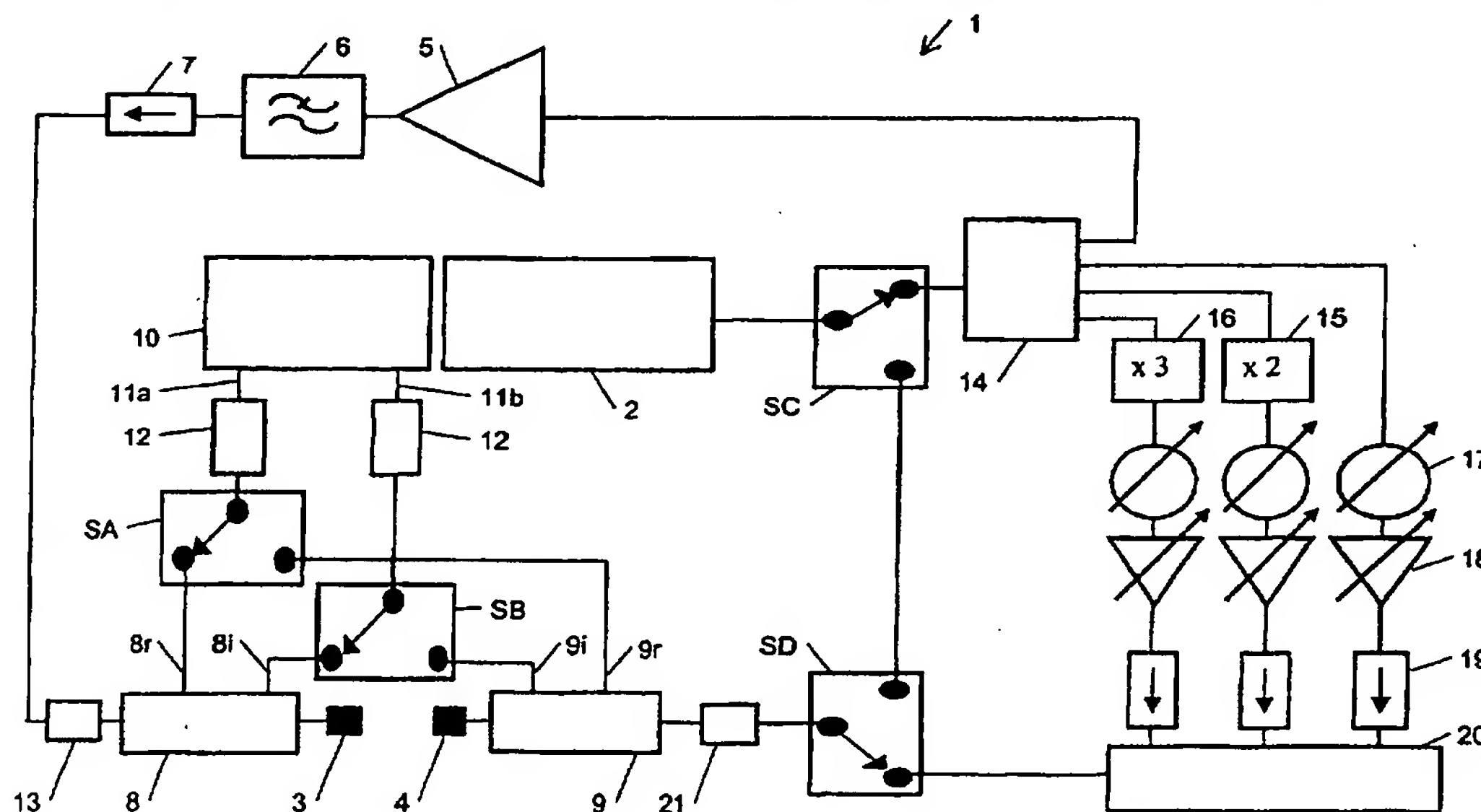
Fig. 1

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High Frequency Circuit Analyser

The present invention relates to analysing the behaviour of a high frequency device, in particular, a high
5   power high frequency amplifier, such as an amplifier for use in a mobile telephone network base-station. The invention also relates to a method of improving the performance of such a device.

It is desirous to improve the efficiency and power
10   capabilities of amplifiers for use in mobile communication base stations and therefore also to provide a design tool for designing such amplifiers. One possible method of improving the design of such amplifiers includes conducting a theoretical analysis of terminal voltage and current
15   waveforms with the aim of analysing and improving the modes of operation of the amplifier required for high efficiency, linearity and power. The behaviour of such amplifiers, being non-linear over much of their operating range, is rather complicated and difficult to define accurately. Such
20   theoretical analysis is therefore generally inadequate when seeking to characterize the behaviour of an amplifier with sufficient accuracy to enable its performance to be improved.

Experimental measurement and analysis of waveforms
25   (including RF load lines, for example) would not of course suffer from the disadvantages associated with theoretical analysis. However, measurement systems of the prior art are generally unable to measure the behaviour of such amplifiers over a sufficiently wide power band at sufficiently high
30   frequencies. Measurement systems having such power and frequency ratings tend to be prohibitively expensive, inefficient and/or do not provide sufficient data to facilitate the improvement of the design of circuits

incorporating the device under test. In particular, one measurement method of the prior art that is able to characterise the behaviour of such amplifiers, the method including using a measurement system based on a vector
5   network analyser (VNA), is able only to provide limited data concerning the linear behaviour of the amplifier. That prior art method is not able to provide any data concerning absolute values relating to the power and relative phase of waveforms outputted by the amplifier in response to input
10 waveforms of known frequencies nor is it a straightforward matter to obtain useful information concerning the non-linear behaviour of the device.

Some of the above-mentioned disadvantages may be mitigated by calibration methods. System calibration
15 procedures for 2-port measurement systems have been developed since the beginning of automated network analysis in the late 60's and many known calibration procedures, which allow different levels of accuracy depending on the desired application, are now available. Such calibration
20 procedures are performed with the aim of improving accuracy and creating a well-defined measurement reference plane. However, most established prior art calibration procedures suffer from the disadvantage that they operate on s-parameters, which are defined as travelling wave ratios. As
25 a consequence, only relative measurements are calibrated and absolute power and phase information of incoming and outgoing waves remain undetermined.

A recently proposed measurement system which also seeks to address the disadvantages associated with the prior art
30 is built around two synchronized microwave transition analysers (MTAs)(providing four input channels for measuring the incident and reflected waveforms at each of the two ports of the device under test), with calibration based on

the availability of a multi-tone reference generator, which has an accurately known output impedance, and in respect of which the absolute amplitudes and relative phases of all frequency components are stable and accurately specified.

5 The reference generator is itself calibrated by a broadband accurate signal analyser, using a 'nose-to-nose' procedure (where the reference generator is linked directly to the signal analyser). Obtaining data regarding the behaviour of a device with a system that is calibrated by using a multi-

10 tone reference generator and a broadband accurate signal generator is however very expensive.

The present invention provides a method of measuring the response of an electronic device to a high frequency input signal, the method comprising the steps of:

15 a)   providing an electronic device having a first port and a second port, the ports being able to receive and/or send high frequency signals,

b)   providing a measurement system including a measurement unit having at least two inputs for measuring high frequency

20 signals, and including signal paths able to connect the inputs of the measurement unit to the first and second ports of the device,

c)   applying one or more signals to the device, measuring with the measurement unit via the signal paths two

25 independent waveforms from the first and/or second ports of the device,

d)   switching the signal source to which an input of the measurement unit is connected whilst using the signal at a different input of the measurement unit to maintain a time

30 reference, and

e)   processing signals representative of the waves as measured by the measurement system, with the use of calibration data, to compensate for the influence of the

measurement system on the waves between the first and second ports of the device and the measurement unit and to produce output signals from which the absolute values of the magnitude and phase of waveforms at the first and/or second

5   port of the device may be ascertained.

Thus, the accurate measurements of magnitude and phase of the travelling waves at the measurement reference plane at the ports of the device, including their phase relative to each other, is facilitated by the invention. The

10   absolute voltage and current waveforms at terminals of the device may also be ascertained.

The signal switching step of the method may be performed as follows: at one moment the two inputs to the measurement unit may be sourced from incident and reflected

15   waves at a first port of the device, and then (whilst using the reflected wave input to retain a time reference) the input of the measurement unit relating to the incident wave at the first port is switched to relate to the incident wave at a second port of the device, and then (whilst using the

20   incident wave input to retain a time reference) the input relating to the reflected wave at the first port is switched to relate to the reflected wave at the second port.

A further method of calibration of the prior art is described in a paper entitled "High Power Time Domain

25   Measurement System with Active Harmonic Load-Pull for High Efficiency Base Station Amplifier Design" published in December 2000 in IEEE Transactions on Microwave Theory and Techniques (Vol. 48, No. 12 – publisher identification number S 0018-94800(00)10737-9), the contents of which are

30   incorporated herein by reference. The measurement system described therein is in the form of an Microwave Transition Analyser (MTA) having two inputs. In order to obtain useful data regarding a two port device to be tested it is

necessary to obtain absolute measurements of waveforms at
each port. However, the paper does not provide any means by
which the phase information relating to one waveform can be
compared with another waveform, especially when the signal
source to which the inputs of the MTA are connected are
switched from one port of the device under test to another.
The present invention allows such information to be
ascertained with a single two input measurement unit.

    The method of the present invention is of particular
application in the case where the signals measured by the
measurement unit are converted from high frequency waveforms
to low frequency waveforms. For example, the measurement
system may measure the waveforms by means of combining the
input signal with a comb signal. The comb signal may be at
a frequency significantly lower than the fundamental
frequency of the input waveform. Such a combination may
result in the voltage of the waveform effectively being
measured at successive points along the waveform, the
waveform for example being sampled once every n periods of
the waveform. (It will be appreciated however that such
measurement techniques may rely on the shape of the waveform
changing at a much slower rate than the time required by the
measurement technique to obtain an accurate representation
of the waveform.)

    Preferably, the measurement system further includes a
switching circuit enabling the source of signals received at
at least one input of the measurement unit to be selected.

    The method is of particular application when the number
of absolute waveforms required to be ascertained in order to
characterise sufficiently the device to be tested is greater
than the number of inputs of the measurement unit. For
example, the device to be tested may be a two port device,
such as a transistor, thereby requiring four waveforms to be

measured and calibrated, whereas the measurement unit may only have two inputs.

Conveniently, the independent waveforms measured are two waveforms selected from the group consisting of reflected waveform, incident waveform, current waveform and voltage waveform.

The method may be performed so that the calibration data is retrieved from a data store. The calibration data may be ascertained by performing a series of calibration steps. The method may thus include steps in which a measuring unit, such as the measurement system, is used to ascertain the calibration data by performing one or more calibration steps. Once ascertained, the calibration data is preferably stored in a data store for subsequent use. The calibration data may include first calibration data that may be used to compensate for the influence of the measurement system on the waves between the ports of the device and the measurement unit. Preferably, the first calibration data is such that it would be possible with the data to produce transformed signals, the transformed signals being representative of a function of waves at the first and/or second port of the device. The first calibration data may be used in a calculation that effectively translates the measurement reference plane (i.e. the point or region of the circuit at which the signals as measured accurately represent the form of the waveform) from the measurement unit to the ports of the device. The ports of the device may simply be the leads of the device at their point of exit from the package of the device (for example, the terminals of the device).

The calibration data may include second calibration data. The second calibration data may be such that it could be used to process said transformed signals (see above) to

produce said output signals. The second calibration data may have been ascertained by means of measuring under a plurality of conditions the behaviour of a real network connected to the measurement system. The real network may

5 simply be in the form of a circuit able to carry waveforms from a first point to a second point. Of course the real network will normally have an influence on the waves so carried. The real network may include a part to which a plurality of standards may be applied to produce the

10 plurality of conditions. The real network may include a part at which the behaviour of the real network in response to those conditions may be measured. The real network may also include at least a portion of the measurement system, the portion for example including a connector to which a

15 port of a device to be tested may be connected. Measuring the behaviour of a real network may include providing a connection between a measuring unit, for example the measurement unit, and a connector for connecting to the port of the device, measuring waveforms at the connector via the

20 connection, ascertaining the influence of the connection on the measurement of the waveforms, and then processing the measured waveforms to produce signals representative of the waveforms at the connector. The waveforms measured and processed are conveniently voltage waveforms. The

25 connection may be a part of the analyser. The connection is preferably a passive component. The connection is preferably shielded so that external effects do not have a significant influence on the waves travelling along the connection. The connection may be provided separately from

30 the measurement system. The connection may be in the form of a lead, cable or the like. The connection may for example be in the form of a coaxial cable. The connection may, if a device is present, connect an input of the

measuring unit directly to a port of the device. The ascertaining of the influence of the connection on the measurements made may require calibration of the connection. Such a connection calibration may test a plurality of

5   conditions of the circuit including the connection. For example, the connection calibration may include a short-open-load calibration (see below for further details). The connection calibration may be considered as effectively translating the measurement reference plane from the end of

10   the connection at which measurements are made to the other end of the connection.

Calibration data regarding the measurement system may be ascertained and used in various ways. For example, the ascertaining and use of calibration data may involve the use

15   of an error model representing how signals (for example waves) or variables (for example, s-parameters) derived from such signals are affected by the measurement system. The error model may be a mathematical model involving a plurality of parameters. At least the majority of the error

20   parameters are preferably independent of the port to which the input signal is applied and the port at which the measurements are made. However the error model may include two parameters that allow account to be taken of the influence of the choice of ports (for example when source

25   switching). The error model used is preferably independent of system terminations.

The signals representative of the waves measured by the measurement system may be in the form of data, for example data representative of s-parameters or vector corrected s-

30   parameters. The processing of the signals using the calibration data may make use of an error model at least partly defined by a plurality of error parameters. The method may include a step of ascertaining calibration data

including a step of ascertaining the values of the error parameters of the error model. The error parameters may be ascertained by any suitable method. For example, the measurement system may be tested under controlled
5   conditions, for example such that reflected and/or transmitted waveforms are set to zero, or to other such values that enable the error parameters to be derived. For example, the device may be tested under any of the following sequences of conditions: short-open-load-through (SOLT);
10 through-match-reflect (TMR); or through-reflect-line (TRM). Such calibration conditions are standard and well known in the relevant art. Briefly, the conditions can be explained as follows:

"short"   -   short circuit
15 "open"   -   open circuit
"load"   -   a load is applied across the circuit
(normally the characteristic impedance at the
relevant frequency)
"through" -   used in two port calibrations wherein
20   the two ports are directly connected to each
other
"match"   -   identical to load condition when the
characteristic impedance is applied
"reflect" -   a load is applied across the circuit, the
25   impedance not being equal to the
characteristic impedance
"line"   -   a well defined length of signal path is
connected, the signal path having the
characteristic impedance, the length being
30   selected in view of the wavelength of the
signal applied.

There may be a step in which the second calibration data is ascertained by measuring signals at a port of the device.

The transformed signals (mentioned above) may be representative of vector corrected s-parameters. In that case the second calibration data advantageously relates those s-parameters to the incident and reflected voltage waveforms at the port of the device.

The output signals may relate to, or be calculated from, incident and reflected voltage waveforms at the port of the device to be calculated. The calibrating steps may be performed in such a way that scaling parameter data is ascertained, for example by the measuring of the behaviour of the real network, the scaling parameter data being sufficient to enable the incident and reflected voltage waveforms at the port of the device to be calculated from vector corrected s-parameters relating to the waves at the port of the device.

The device may have more than two ports able to receive and/or send high frequency signals. Of course, if a device has more than two ports, the method may be performed in respect of two or more of the ports, but not all of the ports.

The step of applying a signal to the device is conveniently applied at one of the ports of the device. The step of applying a signal to the device and the step of measuring the resulting incident and reflected waves may be conducted in respect of the same port of the device or in respect of different ports of the device. Signals are advantageously applied such that a plurality of signals are applied having different fundamental frequencies so as to assess the behaviour of the device over a range of frequencies. Preferably, the measurements are made in

respect of a multiplicity of respective applied signals having different fundamental frequencies. The fundamental frequencies of the applied signals in respect of which the behaviour of the device is assessed preferably include a

5 multiplicity of frequencies in the range between 500MHz to 12.5GHz and more preferably include a multiplicity of signals evenly distributed over at least a significant part of that range.

The signal(s) applied to the device preferably include

10 a signal having a fundamental frequency greater than 500MHz.

Reference is made herein to the processing of signals. It will be understood that the signals being processed may be in the form of analogue signals, such as voltage and/or current waveforms, or may be in the form of digitised data

15 representative of such waveforms. As such the method may make use of one or more analogue to digital converters.

The method of the invention is of particular application when the device is a non-linear device, especially where the device is to be used in an application

20 where the operating range of the device is such that non-linear behaviour is significant. A non-linear device is such that the relationship between the output voltage and the input voltage is not linear. The non-linear device may for example be a diode, a mixer, an oscillator or a

25 frequency multiplier such as a doubler, or an amplifying device such as a transistor. The device may be a high power device. The device may be a high power amplifier. The device may for example be a device suitable for use as a high power amplifying device in a mobile telecommunications

30 base station. In such cases, the method advantageously includes a step of applying a high power signal to the device. Such high powers may, depending on the device concerned, be greater than 5W or may be greater than 10W.

The measurement unit advantageously is able to measure and characterise the waveform substantially fully across the time domain. The measurement unit is preferably able to measure accurately waveforms having fundamental frequencies over a frequency range between 500Mhz and 12.5GHz. Of course, the measurement unit may also be able to measure signals having frequencies outside this range. The measurement unit is preferably able to measure high voltage waveforms having fundamental frequencies above 500Mhz. The measurement unit is advantageously a microwave transition analyser (MTA).

The method may include a step of applying a waveform to the device, the waveform having a plurality of single frequency harmonic components. The waveform may, for example, include a component having a fundamental frequency at a first frequency and a component having a second frequency substantially equal to an integer multiple of the first frequency.

The method advantageously includes a step in which signals are simultaneously applied at both ports of the device. In such a case the method may include a step of applying a first waveform at one port of the device, the first waveform having a fundamental frequency at a first frequency and a step of applying a second waveform at another port of the device, the second waveform having a component having a frequency substantially equal to the first frequency and having a component having a frequency substantially equal to an integer multiple of the first frequency. Signals applied to the device may include a combination of signals at the first frequency, and at least the second (twice the first or fundamental frequency) and third (three times the first or fundamental frequency) harmonic frequencies. The first frequency may be provided

at a power more than twice as great as the power of each of
the harmonic signals. The relative phases of the frequency
components of the signals applied to the device are
advantageously accurately pre-selectable. The magnitudes of
5   the frequency components of the signals applied to the
device are advantageously accurately pre-selectable. For
example, there may be provided a first frequency generator
able to generate signals at a first frequency at powers up
to 200W (rms), a second frequency generator able to generate
10   signals at a frequency of twice the first frequency at
powers up to 40W (rms), and a third frequency generator able
to generate signals at a frequency of three times the first
frequency at powers up to 40W (rms).

Each signal path between the measurement unit and the
15   device preferably includes an attenuator, to reduce
reflections at the measurement unit. The incident and
reflected waves may be separated by a directional coupler
connected to the port of the device.

A Bias T device may be provided to combine the high
20   frequency signals with a DC signal for biasing the device.
The high frequency signals may be produced by a signal
generator including a signal amplifier. At least one
isolator may be provided between such a signal amplifier and
a port of the device to isolate the signal at the desired
25   frequency.

The method is of course of particular advantage when
the absolute values of the magnitude and phase of waves at
the port of the device are directly ascertained. The method
thus preferably includes a step in which the absolute values
30   of the magnitude and phase of waves at the port of the
device are directly ascertained.

The time delay between applying the signals and
producing the output signals may be less than 1 minute and

is preferably less than 10 seconds. The method preferably includes producing the output signals substantially in real-time. The method preferably includes producing output signals in a form able to be viewed by an operator, for example by producing a graphical output on a visual display unit, such as a computer monitor, for example.

Features described above may of course be combined where appropriate.

The present invention also provides, according to a second aspect of the invention, a waveform analyser for measuring the response of a two port electronic device to a high frequency input signal, the analyser including:

two device input connections for connecting to ports of a device to be analysed,

a measurement system including a measurement unit and signal paths for connecting inputs of the measurement unit to the device input connections, the analyser being so arranged that the measurement unit is able to measure in use via the signal paths independent waveforms from the ports of a device connected to the device input connections,

a switching circuit able in use to switch the signal source to which an input of the measurement unit is connected,

a signal generator able in use to send high frequency signals to a port of a device to be analysed,

a processor arranged to receive output signals from the measurement system, and

a data store for holding data accessible by the processor, wherein

the processor is programmed to be able, in use of the analyser:

to maintain a time reference using a signal resulting from one of the inputs of the measurement

unit, whilst the source to which another input of the measurement unit is connected is being switched by operation of the switching circuit,

to access calibration data held in the data store,

5   to process data resulting from the output signals from the measurement system received by the processor, the data being representative of waves as measured by the measurement system,

to compensate, with the use of the calibration

10   data, for the influence of the measurement system on the waves between the first and/or second port of the device and the measurement unit, and

to produce output data from which the absolute values of the magnitude and phase of waveforms at the

15   first and/or second port of the device may be directly ascertained.

An active harmonic load pull may be provided by a first frequency generator able to generate signals at a first frequency and at least one further frequency generator able

20   to generate signals at a different frequency. For example, there may be provided a first frequency generator able to generate signals at a first frequency, a second frequency generator able to generate signals at a frequency of twice the first frequency and a third frequency generator able to

25   generate signals at frequency of three times the first frequency.

An active harmonic load-pull may be applied at high power levels, preferably over 10 Watts (rms), and more preferably over 20 Watts (rms). The analyser may include

30   one or more signal generators able collectively to produce an active harmonic load-pull at power levels up to at least 30 Watts (rms).

At least a part of the processor may be in the form of a suitably programmed computer. The processor is preferably in the form of a computer, such as a suitably programmed stand alone computer, or in the form of a dedicated

5   processor. A separate processor for calibrating may be provided.

The signal generator may be formed of many separate components including for example one or more of the group consisting of a single frequency signal generator, a signal

10   splitter, a signal amplifier, a multiplexer or signal combining means, a phase shifter, and a frequency multiplier. The signal generator may be able to produce an accurately definable waveform being a combination of one to ten simple harmonic waveforms.

15   The waveform analyser according to the above-described second aspect of the present invention is preferably so configured as to be able to perform the method of the present invention according to the first aspect of the invention herein described. Also, the method of the present

20   invention according to the first aspect of the invention herein described may be performed using a waveform analyser according to the second aspect of the present invention. For example, the analyser may be suitable for measuring devices having more than two ports.

25   The present invention also provides according to a third aspect of the invention a method of improving the design of a high power high frequency electronic circuit, the method including the steps of measuring the device by means of a method according to the first.aspect of the

30   invention or by means of the use of a waveform analyser according to the second aspect of the invention. The design may for example be improved by outputting data relating to current and voltage waveforms outputted by the device,

varying harmonic loads on the device, and then analysing the outputted data relating to current and voltage waveforms to assess the loads that facilitate the better performance of the device. An improved high power high frequency

5   electronic circuit including the device, may then be designed in consideration of the results of the analysis so performed.

The performance of the circuit may for example be improved by improving one or more of the efficiency, gain,

10   or maximum power output of the circuit. The circuit may be improved in design by varying the bias point or drive level of the device, or by varying the harmonic tuning of the circuit. According to a fourth aspect there is also provided a method of manufacturing a high power high

15   frequency electronic circuit, the method including the steps of designing the circuit in accordance with a method according to the third aspect of the invention and manufacturing the high power high frequency electronic circuit so designed. The circuit may be a signal amplifier.

20   The device may be a transistor.

The present invention also provides in accordance with a fifth aspect a method of manufacturing a high power high frequency circuit including an electronic device, the method including the steps of analysing the device by performing a

25   method according to the first aspect of the invention or by using an analyser according to the second aspect of the invention and then tuning the circuit in response to the results of the analysis so performed.

An embodiment of the invention will now be described,

30   by way of example only, with reference to the accompanying schematic drawings of which,

Fig. 1   shows a schematic circuit diagram of an

analyser for analysing a 2-port LDMOS
device;

Figs. 2a and 2b   show error models used in a calibration
of a measurement system of the analyser;

5   Fig. 3   shows a modified error model after
insertion of a coaxial cable for
performing a power calibration step;

Fig. 4   shows a complete system error model for
a waveform vector correction method used
10   in the method of the embodiment;

Fig. 5   shows a small signal model topology
adopted for the device;

Fig. 6   shows extrinsic and intrinsic efficiency
load-pull contours as measured by the
15   analyser;

Fig. 7   is a graph showing RF load lines at
increasing input power into optimum
fundamental load, together with measured
DC output characteristics;

20   Fig. 8   is a graph showing harmonic powers at
increasing input power into optimum
fundamental load;

Figs. 9a and 9b   are graphs showing measured waveforms at
an output current generator before and
25   after harmonic tuning for efficiency;

Fig. 10a and 10b   are graphs showing measured waveforms at
an output current generator before and
after waveform engineering;

Fig. 11   is a graph showing measured waveforms at
30   an output current generator after
waveform engineering and 2dB increase in
drive level; and

Fig. 12   is a graph showing RF load lines
                               measured at a given voltage and current.

        Figure 1 shows a schematic circuit diagram of an
5   analyser 1 for measuring the response of an electronic
     device (hereinafter device under test or DUT) to a high
     frequency and high power input signal (the DUT is not shown
     in Fig 1). The analyser 1 has time domain high power
     testing capabilities and is also able to apply an active
10   load-pull involving three harmonics to the device under
     test. The analyser 1 is based on a two channel sampling
     oscilloscope and test set. The analyser 1 comprises a
     synthesized sweeper source signal generator 2 connected to
     two ports 3, 4 to which a DUT (not shown) is attached. The
15   DUT is a 2-port LDMOS packaged device mounted on a
     microstrip-based fixture. The source signal is directed to
     either port 3, 4 by two switches SC and SD. A 200W solid-
     state drive amplifier 5 for amplifying signals at a
     fundamental frequency, is connected to the first port 3 via
20   a low-pass filter 6, provided to suppress any harmonic
     content generated by the drive amplifier 5, and an isolator
     7, for isolation at the fundamental frequency. The drive
     amplifier 5 has a frequency bandwidth of 1.8 to 2.0GHz.
        The active load pull capability of the analyser 1 is
25   provided by an active harmonic load-pull circuit implemented
     to have a feed-forward architecture. A four-way power
     splitter 14 provides four fundamental frequency signals of
     which one is fed to the drive amplifier 5 (mentioned above).
     Of the other three signals, one is used directly to actively
30   load pull the DUT at the fundamental frequency. A frequency
     doubler 15 and a frequency tripler 16 provide a second
     harmonic signal component and third harmonic signal
     component for the active harmonic load pull. All three

signal components can be changed individually in phase (by phase shifters 17) and magnitude (by variable amplifiers 18) allowing the resulting three harmonic loads to be set anywhere on the Smith chart. The three signals, after each

5   signal has passed through its respective phase shifter 17 and variable amplifier 18, pass via respective isolators 19 (in order to reduce or remove any external effects due to unwanted signals in the circuit), and are then combined by a triplexer 20. The maximum output powers of the solid state

10 variable amplifiers 18 determine the maximum magnitude of the load pull signals. In the present embodiment the power ratings are 200W at the fundamental frequency and 40W at the second and third harmonic frequencies. The active load pull circuit is connected to the second port 4, via a Bias-T

15 device 21 and a sensing coupler 9 (described in further detail below). The system configuration is such that packaged devices may be tested and load-pull measurements may be performed up to a 30W output power level.

In order to characterise a two-port device it is

20 necessary to analyse four parameters. The analysis of the four parameters in this embodiment involves measuring the incident and reflected waveforms at each of the two ports 3, 4 connected to the DUT. Two directional couplers, 8, 9, one connected to each port 3, 4, act on waveforms at the ports

25 3,4 to produce signals (at outputs 8i, 8r, 9i, 9r of the couplers) split into incident and reflected waves, thereby producing four coupled waveforms. A microwave transition analyser 10 (MTA) has two input channels 11, which receive two of the four coupled waveforms via switches SA and SB.

30 Switch SA determines which of i) the de-coupled incident waveform at the first port 3 and ii) the de-coupled incident waveform at the second port 4 is forwarded to the first input channel 11a of the MTA 10. Switch SB determines which

of i) the de-coupled reflected waveform at the first port 3
and ii) the de-coupled reflected waveform at the second port
4 is forwarded to the second input channel 11b of the MTA
10.

5   However, in order to produce output data with relative
phase information regarding the waveforms it is necessary to
maintain a constant time reference between the waveforms
measured by the MTA 10 (at the two input channels of the
MTA). When switching between inputs to the MTA 10 by
10   switches SA and SB it is therefore necessary to maintain a
time reference. When switching from two waveforms of the
four waveforms to be measured to the other two waveforms,
the switches must be activated one at a time. For example,
at one moment (the situation shown in Fig. 1) the switches
15   SA and SB are set so that incident and reflected waves are
sourced from the first port 3. In order to change the
inputs received by the MTA 10 to be those sourced from the
second port 4, it is necessary perform the following steps:
        using the reflected wave input from the first port 3
20   (signal 8r) to retain a time reference, switch SB is
switched so that input channel 11b of the MTA 10 receives
the incident waveform from output 9i of the coupler 9 at the
second port 4; and
        then whilst using the incident wave input received at
25   channel 11b from output 9i of the second port 4 as a time
reference, the input relating to the reflected wave at the
first port 3 (output 8r) is switched by switching switch SA
so that the input at input channel 11a of the MTA 10 relates
to the reflected wave at the output 9r of the coupler 9 at
30   the second port 4. Thus the reflected and incident signals
are able to be switched from one port 3, 4 to another 3, 4
without losing the time reference.

Each channel 11 of the MTA 10 has a microwave sampler able to measure the voltage of the waveform at a given instant. Attenuators 12 are inserted in front of each input channel 11 of the MTA 10 to avoid saturation of the MTA 10. The MTA 10 measures the voltage values of the coupled signals in the time domain through a sampler based broadband down-conversion technique resulting in the incoming high frequency signal being converted into a lower frequency signal (the incoming high frequency signal is assumed to be substantially periodic). The resulting low frequency signal is then digitised by an analogue-to-digital converter (ADC) (not shown). The measured incident and reflected voltage waveforms, Vi and Vr, are directly related to the a- and b-travelling waves, and Z_0 (the characteristic impedance) by equations (1) and (2) shown below:

$$\vec{a} = \frac{\vec{V}^i}{\sqrt{Z_0}} \qquad (1)$$

$$\vec{b} = \frac{\vec{V}^r}{\sqrt{Z_0}} \qquad (2)$$

A processor (not shown) calculates s-parameters by taking the ratio of only the fundamental components (calculated by a Fourier transform) of the a- and b-waves (i.e. so that s = b/a), as calculated from, equations (1) and (2) above.

The MTA 10 is able to effect measurement of signals ranging from 0.5 to 12.5GHz. A high power bias T device 13 with a bandwidth of 1.3 to 9GHz is provided between the drive amplifier 5 and the first port 3 to facilitate the analysis of the high power characteristics of the device.

The bias T 13 is able to operate effectively up to at least a continuous wave power of 30W and a DC current of 10A.

The waveforms measured by the MTA are of course those received at the MTA via the switches SA, SB, attenuators 12 and the signal paths connecting those components. The waveforms as measured are therefore not an accurate reproduction of the waveforms at the ports of the DUT connected to the first and second ports 3, 4. Thus, a calibration calculation is carried out by the processor in order to compensate for the influence of those components and signal paths on the waveforms between the ports of the DUT and the point of measurement in the MTA 10. Such a step can be considered as effectively shifting the measurement plane form the MTA 10 to the leads of the package of the DUT. The calibration method operates on the s-parameters as calculated by the processor (see above) to produce vector corrected s-parameters by means of a through reflect load (TRL) calibration.

As mentioned above, the active load pull circuit is connected to the second port 4, via the sensing coupler 9, and does not therefore have a significant influence on the characteristic of the path between the second port 4 and the MTA 10, thereby allowing the synthesized load to be applied and measured without requiring any calibration steps to compensate for the influence of the load pull circuit.

The calibration method used to produce vector corrected s-parameters is performed by a processor, which in the present embodiment in the processor of a computer (not shown) programmed with appropriate software (for example, the PC based HP-Basic control software). The calibration to produce vector corrected s-parameters will now be described in detail.

The calibration is based on a reformulation of the conventional 12-term directional error model of a four-sampler measurement system for s-parameter measurements. Conventional error models require two different, but

5   analogous, models to represent the forward and reverse measurement states, each model having its own set of error coefficients to account for source switching issues inherent with non-ideal reflectometers. The error model utilised in the present embodiment is shown in Figures 2a and 2b

10   illustrating the forward and reverse modes respectively. The error model, which is indicated by the dashed box around the DUT (represented by box 22), does not depend on measurement direction or terminations. The error model (in which isolation terms have been omitted for simplicity)

15   fulfils two main criteria required for an error model that can be extended to absolute vector corrected waveform measurements, namely (1) it is non-directional and independent from system terminations and (2) correction at both ports at the same time is possible (i.e. all four

20   reference planes are present in the model).

The error model as shown in Figs. 2a and 2b shows how error parameters (or error terms) e_{nm} relate to the incident travelling waves a_p and the reflected travelling waves b_q. The measured waveforms a_0, b_0 (from the first port 3) and a_3,

25   b_3 (from the second port 4) yield the s-parameters s_0 and s_3. For example, in the forward mode (shown in Fig. 2a) the measured waveforms a_0, b_0 at the input to the MTA 10 depend on the actual waveforms a_1, b_1 at the port of the DUT connected to the first port 3 by the equations $b_0 = e_{00}a_0 +$

30   $e_{01}e_{10}a_1$ and $b_1 = a_0 + e_{11}a_1$ and the s-parameter by the equation $s_{00} = b_0/a_0 = e_{00} + e_{01}e_{10} \Gamma_{DUT} / (1 - e_{11}\Gamma_{DUT})$, where Γ_{DUT} is the reflection coefficient of the DUT 22 (i.e. $\Gamma_{DUT} = a_1/b_1$). In the reverse mode (shown in Fig. 2b), $b_2 = e_{22}a_2 + e_{23}a_3/ e_{10}$ and

$b_3 = e_{32}e_{10}a_2 + e_{33}a_3$, so that the s-parameter $s_{33} = b_3/a_3 = e_{33} + e_{23}$ $e_{32} \Gamma_{DUT} / (1 - e_{22}\Gamma_{DUT})$, where Γ_{DUT} is the reflection coefficient of the DUT 22 (i.e. $\Gamma_{DUT} = a_2/b_2$).

The MTA 10 is configured in such a way that the measurements thereby made are, internally calibrated if necessary, so that the influence of the MTA 10 on the measurements made do not need to be accounted for. Apart from terms relating to the source switch non-idealities (the two match error terms Γ_0 and Γ_3), the error model is symmetrical and only one set of error terms need define the system in both forward and reverse modes. The two match error terms Γ_0 and Γ_3 can be simply measured during calibration by configuring the system source switch to run the directional couplers 8, 9 backwards. For example during the standard through line forward measurement, inverse e_{33}, obtained by measuring $1/e_{33}$ while sourcing from port 1 (forward), gives the ratio a_3/b_3, which is the wanted source switch match Γ_3. The error parameters of the error model are ascertained by a Through-Line-Reflect (TLR) calibration, under the control of the software. Other calibration methods, such as Short-Open-Load-Through (SOLT) and Through-Match-Reflect (TMR), could also be used to ascertain the error parameters.

The resulting error model after s-parameter calibration can simply be extended for absolute magnitude and phase correction of the travelling waves, through a further calibration step, which will be referred to as 'power calibration', which determines the scaling parameter e_{10}. The response coefficient e_{10} is equal to the ratio a_1 / a_0 (see Figs. 2a, 2b and 3) and is ascertained by effectively measuring with the MTA the wave magnitude and phase at the reference plane at the port of the DUT connected to the first port 3. The actual measurement is performed by

attaching a coaxial cable from a port of the MTA 10 and then
the processor translates the measurement reference plane
from the MTA 10 to the relevant port of the DUT.

In order to perform such a translation the cable (not
5   shown) need to be calibrated. After inserting a through
line between the two measurement ports 3, 4, a cable (not
shown) is connected at the end of the directional coupler 8
connected to the first port 3. (Alternatively the cable
could be connected to the load switch SD.) A one port
10   Short-Open-Load calibration is then performed at the free
end of the cable, the MTA 10 measuring the resulting
incident and reflected waveforms via either or both the
couplers 8, 9. The calibration so performed allows the
processor to compensate for the influence of the cable on
15   the measurements made via the cable. Then a through
calibration step is performed by attaching the free end of
the cable to one of the inputs 11a of the MTA 10. The
voltage waveforms at the inputs at the MTA 10 consist of a
waveform from which the voltage waveform at the first port 3
20   may be calculated (because the characteristics of the cable
are now known) and a waveform relating to the voltage
waveform at the second port 4. Because the voltage
waveforms at ports 3 and 4 are identical or are related to
each other by a known relationship (owing to the through
25   connection between the two ports 3, 4), the influence of the
rest of the measurement system (between the second port 4
and the other input channel of the MTA 10) may be
ascertained by the processor.   The processor may then
transform the wave measurements measured at the inputs 11a,
30   11b of the MTA 10 back to the measurement reference plane of
either the first port 3 or the second port 4. Thereafter,
any ratio of waveforms measured from the first or second
ports 3, 4, may be split into absolute waveforms. The

vector corrected s-parameters (the ratio of the voltage at the fundamental frequency of the voltage wave travelling from the first port 3 to the second port 4 to the voltage at the fundamental frequency of the voltage wave travelling

5   from the second port 4 to the first port 3) at the second port 4 are known from the calibration procedure described above. The voltage waveform travelling from the second port 4 to the first port 3 is known by the use of the through measurement using the cable, that voltage waveform being

10   either the denominator or the numerator of the above-mentioned ratio. Thus, the other of the denominator or the numerator may then be ascertained. Therefore, when measuring the behaviour of a device, the processor and the measurement system are able to derive vector corrected s-

15   parameters and incident and reflected waveforms and/or current and voltage waveforms at the second port 4. The same process as described above may be performed in order to enable the same information to be ascertained at the first port 1. Alternatively, the above process may be sufficient

20   to enable such information to be ascertained by means of a mathematical relationship between the first and the second ports 3, 4.

Figure 3 depicts the flow graph of the modified system after insertion of the coaxial cable, and the response

25   parameters (e'_{11}, e'_{21}, e'_{12}, e'_{22}) associated to the network between the first port 3 and the coaxial cable reference plane represented by dashed line 23. Symmetry of the response behaviour of this network is assumed, hence the response parameter e'_{21} can be calculated. At this stage

30   connecting the coaxial cable into the b travelling wave measuring channel of the MTA changes the system topology, allowing for the through measurement of the ratio $\Gamma_T = b_c$ /

a_0. The response error coefficient e_{10} can finally be calculated:

$$e_{10} = \frac{\Gamma_T\left(1 - e_{11}e_{11}'\right)}{e_{21}'} \qquad (3)$$

5

After the coefficient e_{10} has been extracted, since this is the error model scaling factor, the remaining transmission coefficients can be calculated:

10 $\quad e_{32} = e_{10}e_{32}/e_{10} \quad e_{01} = e_{10}e_{01}/e_{10} \quad e_{23} = \left(e_{23}/e_{10}\right)\cdot e_{10} \qquad (4)$

The completely extracted error model, shown schematically in Fig.4, allows absolute magnitude and phase of the travelling waves at the DUT reference planes to be

15 simply de-embedded from the raw measured waves:

$b_0 = e''_{00}a_0 + e''_{01}a_1$

$b_1 = e''_{10}a_0 + e''_{11}a_1$

thus:

20 $b_1 = (e''_{10} - e''_{00}e''_{11}/e''_{01})a_0 + e''_{11}/e''_{01} b_0$

$a_1 = (-e''_{00}/e''_{01})a_0 + 1/e''_{01} b_0$

$\qquad\qquad (5) \qquad\qquad\qquad\qquad (5)$

Also,

$s_{00} = b_0/a_0$

25 $s_{11} = b_1/a_1$

Therefore

$s_{11} = (s_{00} - e''_{00}) / (e''_{11}s_{00} + e''_{01}e''_{10} - e''_{00}e'')$

In the above equations and the attached Figures, error

30 terms relating to Figs. 2a & 2B are distinguished from those relating to Fig. 4 by the use of double inverted commas. For example, e''_{01} relates to Fig. 4 and e_{22} relates to

Figs. 2a and 2B. However, in the present embodiment the values of an error parameter in Fig. 2a, 2b is equal to the value of the corresponding error parameter in Fig. 4. For example $e''_{01} = e_{01}$.

5   Voltage and current time domain waveforms are finally obtained by the processor, through inverse Fast Fourier Transforms (FFT), from all the relevant frequency components of the calibrated travelling waves. The waveforms are then displayed on a visual display unit (such as a computer

10   monitor) in real-time allowing the operator of the analyser 1 to assess the change in the measured data in response to a variation in measurement set up, for example by varying the bias point, the drive power level or device load.

        The method of the above embodiment is performed over a

15   wide frequency range (for example over the range 1GHz to 10GHz) and at a various bias points. For a meaningful interpretation of the results obtained all reactive elements need to be characterized and de-embedded. The s-parameter data of the device, obtained from the same measurement

20   system, allows for the extraction of a simple small signal model, which includes parasitic effects. Fig. 5 shows the adopted model, with the device surrounded by the parasitic effects associated to the package. This model topology achieves reasonable fit of the s-parameter data at various

25   bias points across the region of operation. The values for package reactances and device capacitances, which are utilized in the data analysis that follows, are extracted from s-parameters at the quiescent point of large signal operation ($V_{DS,Q}=26V$ $I_{DS,Q}=260mA$). The measured

30   s-parameters compared favourably with the model results. The extracted parameter values are shown below:

        C_{GPAD} 610fF

C_{DPAD}	440fF
L_G	1.27nH
L_D	1.10nH
L_S	55pH
R_D	1.1Ω
C_{GS}	9.38pF
C_{GD}	144fF
C_{DS}	2.95pF
R_{GS}	2.1Ω
G_{DS}	1.58mS
G_M	350mS
Tau	20ps

The reactive parasitic elements can now be de-embedded from the measured waveforms: hence, shifting the measurement reference planes. The time domain output current and voltage data graphs shown in the figures are shifted to the output current generator plane, so as to illustrate better the intrinsic behaviour of the DUT.

Also, small signal s-parameters obtained from the analyser 1 were compared with measurements performed using an HP8510C machine (available from Hewlett Packard). The degree of correspondence was better than -45dB, thereby validating the ability of the analyser to ascertain with accuracy s-parameters at small signals.

The present embodiment facilitates the improvement of the design of amplifier circuits including a transistor (for example an LDMOS device), by means of analysing the behaviour of the transistor. A comprehensive fundamental frequency load pull investigation has been performed on the such an a LDMOS transistor as the DUT, biased at pinch-off with drain voltage V_{DS}=26V. Figure 6 shows the resulting load pull contours of drain efficiency, both at the extrinsic

package leads plane (dotted lines 24) and after de-embedding at the current generator plane (solid lines 25). For the measurement of the load pull contours the second and third harmonic load were 50Ω at the package leads. Contours

5   generated for output power and power gain show similar behaviour and give similar optimum loads. The optimum output reflection coefficient $\Gamma_{OPT}=(0.78 @ 156°)$ at the package lead plane, resulting in an optimum admittance $Y_{OPT}=(15.8 - j5.2)mS$ at the current generator plane, gave a maximum drain

10 efficiency η=59.5%, output power $P_{OUT}=3.91W$, power gain $G=13.6dB$ and a -1dB compression point of 22.4dBm. A swept input power measurement was performed on the device into this optimum fundamental load. Figure 7 is a graph showing the RF dynamic load lines, the horizontal axis representing

15 drain voltage in Volts, and the vertical axis representing drain current in mA, the self biasing points 26 also being shown in Figure 7. Figure 8 is a graph showing the output harmonic power content at increasing output power levels, the horizontal axis representing input power in dBm, the

20 left vertical axis representing output power in dBm and the right vertical axis representing harmonic power in dBm. The graph of Figure 8 has five plots, plot 27 (circles) represents the fundamental frequency, plot 28 (triangles) represents the first harmonic, plot 29 (squares) represents

25 the second harmonic, plot 30 (inverted triangles) represents the third harmonic, and plot 31 (diamonds) represents the fourth harmonic. As can be seen from the measured RF load lines of Fig. 7, the device has an inherent almost accomplished class B harmonic loading, which is due to the

30 output parasitic network. In particular, the large output capacitance creates almost a short circuit for the harmonics at the output current generator plane.

Harmonic tuning was performed on the device biased in the same bias point applying the fundamental load Γ_{OPT} at the package lead while changing the second and third harmonic load at the current generator plane. The appropriate loads

5 to be applied at the package leads were computed using the small signal model. A drive level of 19.2dBm, backed off by approximately 3 dB from the -1dB compression point, provides a high gain while still having a high harmonic content thus allowing for harmonic tuning. In order to investigate the

10 effect of harmonic tuning on the device, a first measurement involved a 50Ω match at the second and third harmonic frequency at the current generator plane. This measurement resulted in an output power of 2.5W with an efficiency η=47%. Class F loading was investigated next, applying a

15 short at the second harmonic and open at the third harmonic frequency at the current generator plane. The result was an increase in both the output power and efficiency. In order to show how much harmonic loading at constant output power can improve efficiency, V_{DS} was reduced until the device

20 provided the same output power P_{OUT}=2.5W, resulting in efficiency η=59%. This indicates that the increase in efficiency was achieved by squaring the voltage waveform. However, the obtained efficiency, which is far from the theoretical value achievable with three harmonic loads,

25 suggests that the applied loading does not constitute the optimum class F loading. This can be readily verified by looking at the measured current and voltage waveforms. Figure 9a is a graph showing the current waveform 33a and voltage waveform 32a before harmonic tuning and Figure 9b is

30 a graph showing current waveform 33b and voltage waveform 32b after harmonic tuning. It can be seen that the achieved gain in efficiency is due to a slightly more compressed (squared) voltage waveform as well as by a reduction of the

area where high current and voltage values co-exist. These results agree with theoretical considerations that a short at the second harmonic and open at the third harmonic do not always constitute an optimum class F loading.

5   Applying the same traditional harmonic tuning approach to the device at the optimum operating conditions described above, improved overall neither the efficiency (η=59.5%) nor the output power (P_{OUT}=3.91W). It was therefore decided to use directly the time domain waveform data as an alternative

10   load-pull approach, with the aim of engineering the intrinsic current and voltage waveforms in order to improve the device performances. The results are shown in the graphs of Figs. 10a and 10b, depicting output current 33a'and voltage 32a' waveforms before waveform engineering (Fig.

15   10a) and output current 33b'and voltage 32b' waveforms after (Fig. 10b) waveform engineering. While changing the fundamental load in order to increase the peak current, the second harmonic load is varied in order to reduce the dip within the current waveform. This results in an output

20   power increase by 450mW while maintaining the efficiency at η=59.5%. The loading for the third harmonic is then used to square the voltage waveform and to minimize the overlap between the voltage and current. The final current and voltage waveforms, shown in Fig. 10b, were a trade-off

25   between reducing their overlap and increasing the current values in the area of low voltages. Overall, the tuning increased the output power by 800mW (20%), giving in total P_{OUT}=4.71W, without compromising gain and efficiency. The resulting harmonic loads at the current generator plane are:

30   fundamental Γ_{OPT}=(0.535 $\angle$ 156°), second harmonic Γ_{2ND}=(1.0 $\angle$ -57°), third harmonic Γ_{3RD}=(1.0 $\angle$ -158°).

Fig. 10b illustrates both the current and voltage signals having a generally square-shaped waveform, which

explains the increase in output power due to the increased
fundamental current swing but not an increase in efficiency
due to the increased quiescent point of a squared waveform.
The fact that the gain has not changed suggests that further

5   improvement in efficiency and output power could be achieved
by increasing the drive level, but neither the efficiency
nor output power are found to increase significantly with
higher drive level. Besides, a dipping in the current
waveform, shown in Fig.11 for a drive level increased by 2

10   dB, appears while the output power is increased. This
indicates a drive dependent effect, which prevents the
device from reaching its optimum performance.

    In all of Figs. 9a, 9b, 10a, 10b, and 11 the current
(left vertical axis) is in mA, the voltage (right vertical

15   axis) is in Volts, and the horizontal axis is in pico-
seconds.

    It has been found that the recurring current dips with
increasing drive level do not result from the injection of
harmonic components from the drive amplifier 5 or from other

20   device non-linearities in the low-pass filter 6 for example.

    The origin of the current distortion, was identified by
analysing the device for a set of load lines, all measured
at the same drive signal level, namely with $V_{DS,Q}=26V$ and
$I_{DS,Q}=260$ mA. Figure 12 shows the resulting measured RF

25   dynamic load lines on a graph, where the horizontal axis
representing drain voltage in Volts, and the vertical axis
representing drain current in mA.   The corresponding
measured current waveforms present an increasing distortion
for increasing output voltage swing. The output current

30   consists of a real current component, whose dependency on V_{DS}
is defined by the output conductance, and a displacement
current term. Since the voltage waveform does not progress
into the knee region, it was assumed that the

transconductance does not change significantly along the measured load lines. It is believed from measurements conducted with the analyser that the origin of the current distortion observed is caused by non-linear capacitance

5   effects. Therefore, in order to further improve the efficiency of power amplifiers based on LDMOS devices non-linear capacitance will have to be analysed and accounted for.

It will be readily apparent to the skilled person that

10   various modifications may be made to the above-described embodiment without departing from the spirit of the invention. For example, further improvements could be made to the present embodiment such as accounting for non-idealities of the MTA input channels, such as mismatch and

15   asymmetry between the two channels.

Claims:

1. A method of measuring the response of an electronic device to a high frequency input signal, the method
5 comprising the steps of:
   a) providing an electronic device having a first port and a second port, the ports being able to receive and/or send high frequency signals,
   b) providing a measurement system including a measurement
10 unit having at least two inputs for measuring high frequency signals, and including signal paths able to connect the inputs of the measurement unit to the first and second ports of the device,
   c) applying one or more signals to the device, measuring
15 with the measurement unit via the signal paths two independent waveforms from the first and/or second ports of the device,
   d) switching the signal source to which an input of the measurement unit is connected whilst using the signal at a
20 different input of the measurement unit to maintain a time reference, and
   e) processing signals representative of the waves as measured by the measurement system, with the use of calibration data, to compensate for the influence of the
25 measurement system on the waves between the first and second ports of the device and the measurement unit and to produce output signals from which the absolute values of the magnitude and phase of waveforms at the first and/or second port of the device may be ascertained.

30
2. A method according to claim 1, wherein the measurement system further includes a switching circuit enabling the

source of signals received at at least one input of the measurement unit to be selected.

3. A method according to claim 1 or claim 2, wherein the measurement unit has only two inputs.

4. A method according to any preceding claim, wherein the independent waveforms measured are two waveforms selected from the group consisting of reflected waveform, incident waveform, current waveform and voltage waveform.

5. A method according to any preceding claim, wherein the calibration data is retrieved from a data store.

6. A method according to any preceding claim, wherein the calibration data is ascertained by performing a series of calibration steps.

7. A method according to claim 6 when dependent on claim 5, wherein the calibration data so ascertained is stored in the data store.

8. A method according to any preceding claim, wherein the calibration data includes first calibration data that may be used to compensate for the influence of the measurement system on the waves between the ports of the device and the measurement unit, and with which first calibration data it would be possible to produce transformed signals, the transformed signals being representative of a function of waves at the first and/or second port of the device.

9. A method according to claim 8, wherein the calibration data includes second calibration data that may be used to

process said transformed signals to produce said output signals.

10. A method according to any preceding claim, wherein at least a part of the calibration data used has been ascertained by means of measuring the behaviour of a real network under a plurality of conditions resulting from the application of a plurality of standards to the real network, the real network being connected to a portion of the signal path that in use connects to a port of a device to be tested.

11. A method according to any preceding claim, wherein the device is a non-linear electronic device.

12. A method according to any preceding claim, wherein the device is a high power device and the method includes a step of applying a high power signal to the device.

13. A method according to any preceding claim, wherein the measurement unit is able to measure high voltage waveforms having frequencies above 500Mhz.

14. A method according to any preceding claim, wherein the measurement unit is a microwave transition analyser.

15. A method according to any preceding claim, wherein the method includes a step of applying a waveform to the device, the waveform having a fundamental frequency at a first frequency and having a harmonic component at a second frequency substantially equal to an integer multiple of the first frequency.

16.   A method according to any preceding claim, wherein the method is performed so that the output signals are produced substantially in real-time.

5   17.   A method according to any preceding claim, wherein the method is performed so that the output signals are produced in graphical form able to be viewed by an operator.

18.   Waveform analyser for measuring the response of a two
10   port electronic device to a high frequency input signal, the analyser including:

two device input connections for connecting to ports of a device to be analysed,

a measurement system including a measurement unit and
15   signal paths for connecting inputs of the measurement unit to the device input connections, the analyser being so arranged that the measurement unit is able to measure in use via the signal paths independent waveforms from the ports of a device connected to the device input connections,

20   a switching circuit able in use to switch the signal source to which an input of the measurement unit is connected,

a signal generator able in use to send high frequency signals to a port of a device to be analysed,

25   a processor arranged to receive output signals from the measurement system, and

a data store for holding data accessible by the processor, wherein

the processor is programmed to be able, in use of the
30   analyser:

to maintain a time reference using a signal resulting from one of the inputs of the measurement unit, whilst the source to which another input of the

measurement unit is connected is being switched by operation of the switching circuit,

to access calibration data held in the data store,

to process data resulting from the output signals from the measurement system received by the processor, the data being representative of waves as measured by the measurement system,

to compensate, with the use of the calibration data, for the influence of the measurement system on the waves between the first and/or second port of the device and the measurement unit, and

to produce output data from which the absolute values of the magnitude and phase of waveforms at the first and/or second port of the device may be. directly ascertained.

19. A method of improving the design of a high power high frequency electronic circuit, the method including the steps of measuring the device by means of the method of any of claims 1 to 17 or by means of the use of an analyser according to claim 18 outputting data relating to current and voltage waveforms outputted by the device, varying harmonic loads on the device, analysing the outputted data relating to current and voltage waveforms to assess the loads that facilitate the better performance of the device, and designing an improved high power high frequency electronic circuit including the device, the circuit being designed in consideration of the results of the analysis so performed.

20. A method of manufacturing a high power high frequency electronic circuit, the method including the steps of designing the circuit in accordance with the method of claim

19 and manufacturing the high power high frequency
electronic circuit so designed.

21. A method according to claim 19 or 20, wherein the
5   circuit is a signal amplifier and the device is a
transistor.

22. A method of manufacturing a high power high frequency
circuit including an electronic device, the method including
10   the steps of analysing the device by performing the method
of any of claims 1 to 17 or by using an analyser according
to claim 18 and then tuning the circuit in response to the
results of the analysis so performed.

15   23. A method of analysing the behaviour of an electronic
device substantially in accordance with the method herein
described with reference to the accompanying drawings.

24. An analyser for analysing the behaviour of an
20   electronic device, the analyser being substantially in
accordance with the analyser as herein described with
reference to the accompanying drawings.

| Application No: | GB 0128634.3 | | Examiner: | John Watt |
| Claims searched: | 1 - 24 | | Date of search: | 19 September 2002 |

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.T): G1U (UR2702, UR2728, UR3500)

Int Cl (Ed.7): G01R 27/02, 27/28, 35/00

Other: Online: EPODOC, JAPIO, WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
A	US 5434511 (ADAMIAN) see whole document	
A	US 5117377 (FINMAN) see col.1, lines 40 - 52 and col.2, lines 43 - 65	
A	US 5097215 (EUL ET AL) see col.1, lines 8 - 59	
A	IEEE Transactions on Microwave Theory and Techniques Vol.48, No.12, December 2000, J. Benedikt et al "High-power Time-Domain Measurement System...." pages 2617-2624.	

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

Fig. 1

Fig. 2a

Fig. 2b

Fig. 3

Fig. 4

Fig. 5

Fig. 6

Fig. 7

Drain Current [mA]

Drain Voltage [V]

Fig. 8

Output Power [dBm]

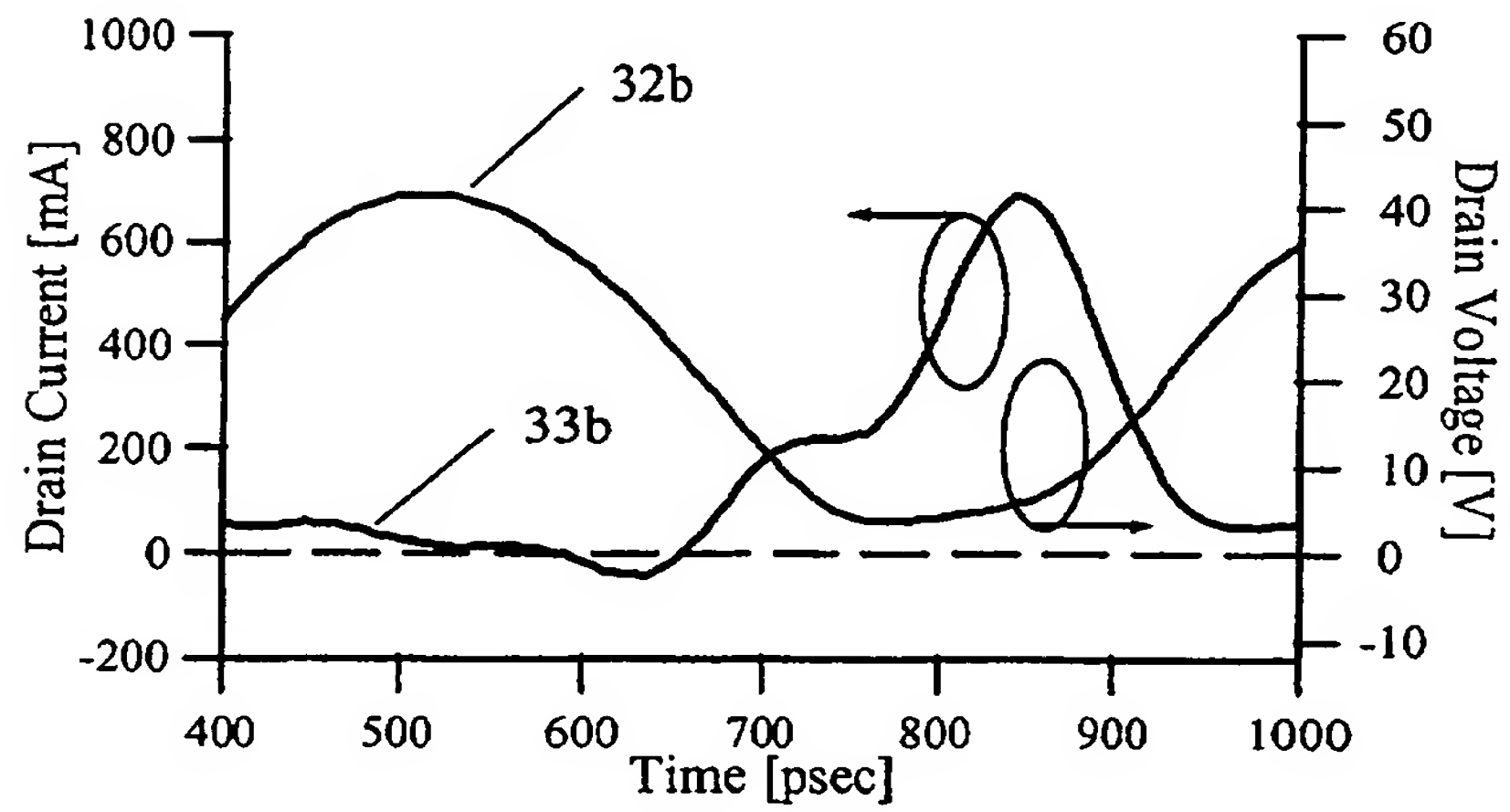Harmonics Power [dBm]

Input Power [dBm]

Fund
2nd
3rd
4th
5th

Fig. 9a

Fig. 9b

Fig. 10a

Fig. 10b

Fig. 11

Fig. 12